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A Low Offset Op-Amp Designed in 180nm Technology

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Abstract—*CMOS op-amps are essential parts in various analog as well as mixed signal circuits and systems. It has widely used in many applications like comparator, integrator, differentiator, filters, zero crossing detector, phase detector, sample and hold circuit, rectifiers, amplifier, oscillator, ADC, voltage follower etc. so designing an Op Amp is a major concern.*

The Two-Stage CMOS Op-Amp has been designed using design specifications and calculated profile parameters of op-amp like Gain bandwidth product, phase margin, power dissipation. The design has been analyzed for different values of the coupling capacitor. In our designed circuit, the first stage provides gain 33 dB and the second stage provides a gain of 34dB. The gain will decrease for larger values of coupling capacitor. Results are compared with two values of input common mode range. Improvement in the designed circuit has done to achieve the desired GBW by recalculating the W/L ratios of transistors and then simulating the results. Desired Gain Bandwidth product of 30 MHz and Phase Margin >60 degrees is achieved but at the cost of power dissipation. There is always a trade-off between the two parameters, i.e. For larger values of GBW, P.M decreases. For Op Amp to operate for High-frequency applications, it is desired to increase the GBW. Design and Simulation are done using UMC 180 nm CMOS technology.

Keywords*: 2 stage CMOS op-am;, cadence virtuoso; design; simulation and result.*

1. INTRODUCTION

CMOS op-amp is the basic structure of different analog and other systems. Its main quality is simple structure and robustness. Due to its these qualities, it mostly uses full circuit system. When an op-amp has designed some electrical characteristics, e.g., gain-bandwidth, common-mode range, slew rate, output swing, offset, all have to be taken into consideration [1]. When op-amp are designed with negative feedback then the main issue is its stability. Stability is the main consideration. It is indicated by phase margin. So for required phase margin compensation for the stability in closed loop system has needed. When comparing the stability and other parameters then other parameters can be compromised [2].

By different methodology an op-amp can be designed but for required specification and stability a particular methodology has been used which fulfills the desired conditions. The need of proposed method is frequency compensation which is achieved by using Miller effect. For that a compensation capacitor Cc has been used between first amplifying stage and second amplifier [3]. Due to the direct path by the capacitor another zero created at the right side of the graph which harms the quality of the phase margin. So there is a need of proper resistor to cover this drawback, for that a resistor is applied in series.

This high value of Cc degrades highly valuable degree-of-freedom for analog system design, like a tradeoff between the power consumption of the circuit and noise of circuit. So this technique highly reduced the value of compensation capacitor than the other techniques. So a large range of the coupling capacitor has achieved and also got highly effective Phase Margin and Gain Bandwidth product.

A. System Overview

For made up the system its basic blocks are needed. All the basic blocks have their own circuits according to requirements The original circuit of each block has the most important in making because it made according to the requirement of parameters and desired output. This topology has designed according to its advantages and disadvantages [5]. The basic block diagram of it is shown below in Fig. 1.

A two stage op-amp basically consists of these main blocks:

1. Amplifiers (A1 and A2)
2. Biasing circuit
3. Frequency compensation circuit.

To propose high noise immune system a Differential pair amplifier has used as input amplifier A1 and for high gain at output stage common source amplifier A2 has been used. The R and C circuit has connected in series with output that is called as RC Miller frequency compensation circuit, and a current mirror circuit is also used [6].

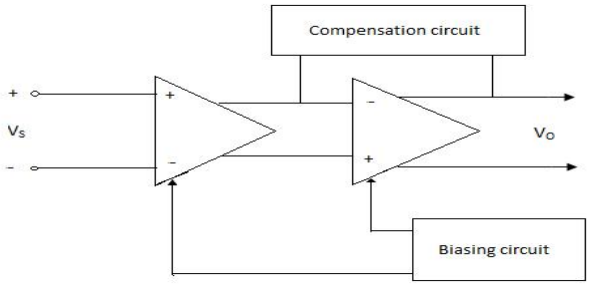

Fig. 1: Basic Block Diagram of a two stage op-amp

2. CIRCUIT DESCRIPTION

A. Amplifiers (A1 and A2) Biasing circuit

The essential function of most of the analog as well as many digital circuits arw Amplification. In this circuit, at first, a differential amplifier (A1) with biasing by a current mirror circuit has been used. Differential amplifier has a large range to avoid the environmental noise. Common source amplifier (A2) is used in the second stage of the two-stage op-amp and because it provides large gain. It means it shows high output swing [7][8].

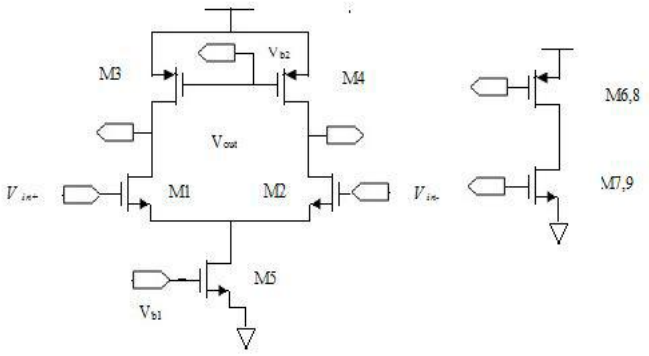

Fig. 2: Two stage amplifiers(i.e. Input and Output)

(i) Differential pair (A1)

(ii) Common Source (A2)

In this M_1 and M_2 is NMOS device that has been used for input, whose transconductance is useful in gain expression. To achieve high gain and Input Common Mode Rejection ratio (ICMR), these devices with required small overdrive voltage has been used. M_3 and M_4 are PMOS devices in with high output resistance for as required high gain. Tail transistor M_5 possess twice as high overdrive voltage as compare to input devices.

B. Biasing circuit

There are many techniques for transistor biasing in IC technology. In earlier voltage biasing was mainly in use. But in these days current biasing is useful for its many advantages over voltage biasing. When using MOS devices in saturation region then it provides constant current (neglect lambda effect) at there. When applying the voltage in metal or semiconductor then electron starts to flow. Similarly a current flow in a metal or semiconductor it produces voltage. This concept is the core of current mirror circuits.

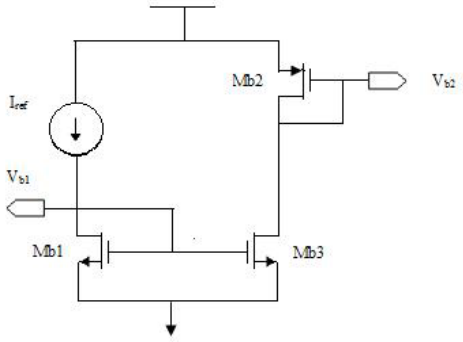

Fig. 3: Current mirror circuit for biasing purpose

In this circuit, the I_{ref} is a current source which is taken as an idle current source. The aspect ratio of NMOS devices Mb1 and Mb3 are decided according to the necessity of bias voltage for M_5, M_7 & M_9 transistors and similarly bias voltage for M_3 and M_4 is created by Mb2. The exactness of the circuit is a key factor for the performance. Its performance is directly proportional to circuit's exactness.

C. Frequency compensation circuit

The negative feedback has been used in circuit at amplifier stage because it is very useful in analog circuit and mix circuit. When an extra amplifier circuit has used in close loop then it gives an extra pole. The order of the location of this extra pole has less than the almost 10 times of dominant pole of initial system, then the phase decreases drastically by this extra pole.

The oscillation decreases the performance of the circuit, so for good performance a high value of phase margin has needed. There are numerous methods to reduce disadvantages of extra poles by frequency compensation. In proposed method a RC miller compensation circuit has been used which change the value of a pole. Miller compensation circuit shift the pole in left of its primary location and according to the circuits other parts values [6]. This technique is described in following points.

Basic purposes –

To nullify the unintentional creation of poles by positive feedback, this will cause the amplifier to oscillate.

To be in command of overshoot and ringing in the step response of the amplifier.

To achieve stable operation, when negative feedback is applied.

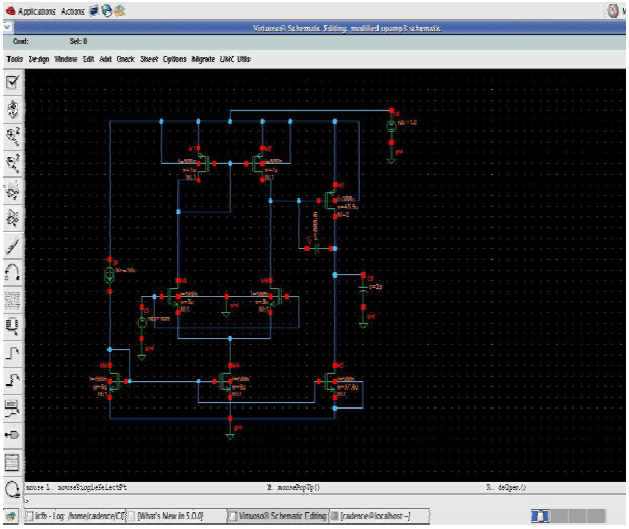

Fig. 4: Designed two stage op-amp

D. Design Equations for two stage op-amp

The differential amplifiers inputs are noninverting(+) and inverting inputs. Noninverting port has the positive value (V+) and inverting input have a negative value(V-) of voltage. So by this circuit, the difference between these two input ports is amplified and the output voltage of the op-amp Vout is given by the equation:

$$V_{out} = A_{OL}(V_+ - V_-) \quad (1)$$

where A_{OL} is the open-loop gain of the amplifier (the term "open-loop" means the gain of the circuit without feedback).

The input signal Vin appears at both (+) and (−) pins, resulting in a current I through Rg equal to Vin/Rg.

where C_c coupling capacitor

the drain current formula in most is

$$I_D = [\mu_{n,p}\, c_{ox}\, (W/L)(V_{eff})^2]/2 \quad (5)$$

Where $\mu_{n,p}$ shows the mobility of MOSFET type,

c_{ox} is the capacitance of the oxide layer and V_{eff} is effective voltage.

$$I_D = [\mu_{n,p}\, c_{ox}\, (W/L)(Vgs-Vt)^2]/2v \quad (6)$$

Where Vgs is gate to source voltage and Vt is threshold voltage of MOSFET

And another formula for transconductance is

$$g_m = d\, I_D / dV_{gs} \quad (7)$$

the relation of output current and drain current is

$$2\, I_d = Io \quad (8)$$

And the most important term DC gain of the circuit is

$$A_{DC} = g_{m1}\, R1 * g_{m2}\, R2 \quad (8)$$

Where g_{m1}, g_{m2} are transconductance of these two stages and R1 and R2 is input side and output side resisters.

And gain bandwidth product has given by

$GBW = gm1/C_C$

Where GBW is gain bandwidth

Kirchhoff's current law shows that the sum of leaving current is equal to the entering current at the same point, which has different paths or leaves. The impedance into the (−) pin is near infinity, so practically it has been known that the entire current I flows through R_f, which create an output voltage.

3. SIMULATION RESULTS:-AT CC= 800FF,

For 0.8V, Gain = 63.64dB (G1 = 33.3dB and G2 = 30.34dB)

For 1.6V, Gain = 58.85dB (G1 = 27.1dB and G2= 38.62dB)

$$V_{out} = V_{in} + i * R_f \quad (2)$$

Where R_f is feedback resistance.

To improve Gain for maximum value of ICMR i.e. at 1.6V, the value of Cc has decreased from 800fF to 500fF.

By combining terms, the determined closed-loop gain A_{CL}:

$$A_{CL} = V_{out}/V_{in} = 1 + R_f/R_g \quad (3)$$

This formula is a basic essential formula for close loop gain. And some basic formulas are given below for our circuit.

For transconductance (g_m)

At Cc= 500Ff,
For 0.8V, Gain = 67.24dB (G1 = 33.28dB and G2 = 33.95dB)

For 1.6V, Gain = 60.55dB (G1 = 27.20dB and G2= 33.34dB)

$g_m = g_b * Cc * 2\pi$ (4)

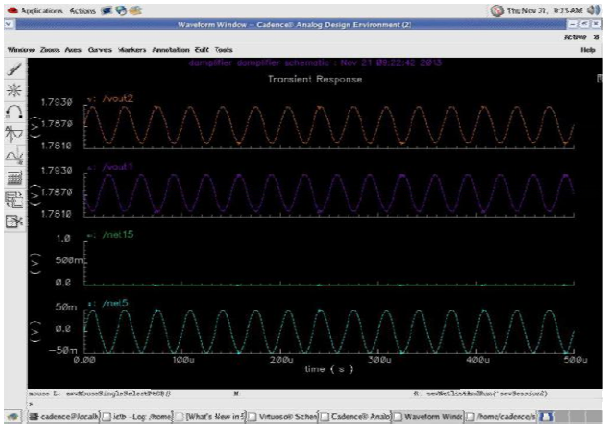

Fig. 5: Transient response of different Amplifier

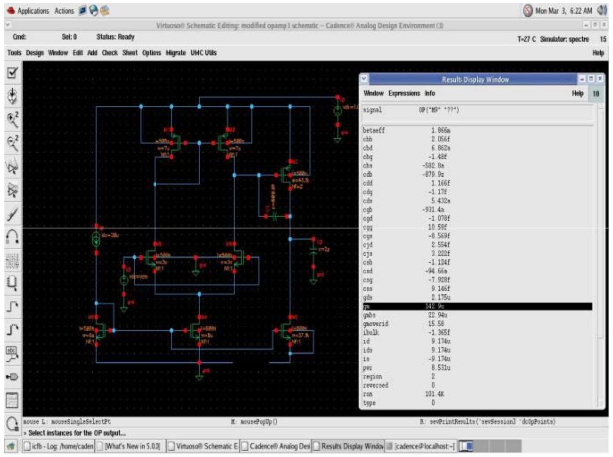

Fig. 6. Two stage op-amp DC analysis

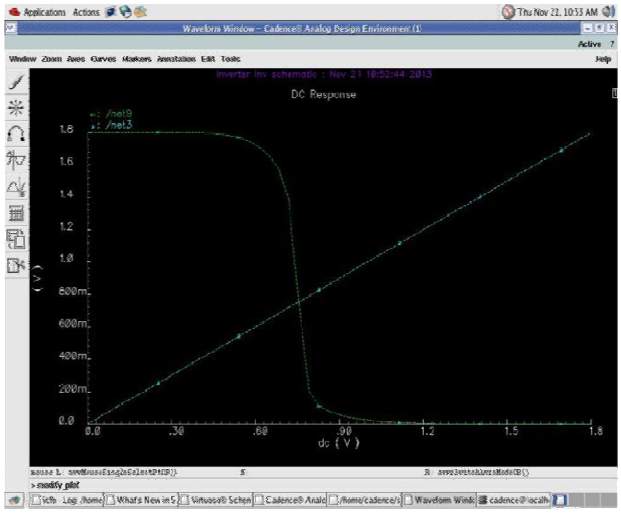

Fig. 7: DC response

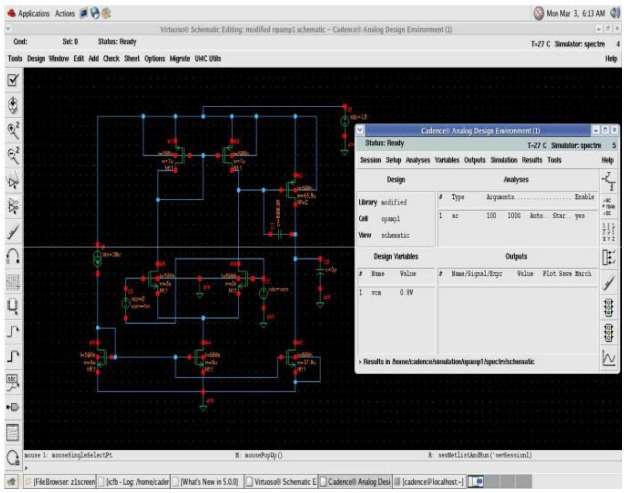

Fig. 8. Two stage op-amp AC analysis

At gain crossover frequency, gain= 0dB and phase margin is calculated.

TABLE 1: Gain for different coupling capacitor

Coupling Capacitor(Cc)	Gain	
	0.8V	1.6V
800f F	63.64dB	58.85dB
500f F	67.24dB	60.55dB

At 0dB gain, the value of GBW product has been measured which is equal to the gain crossover frequency eg. 22.81 MHz and at this frequency the calculated phase margin = 66.87 º

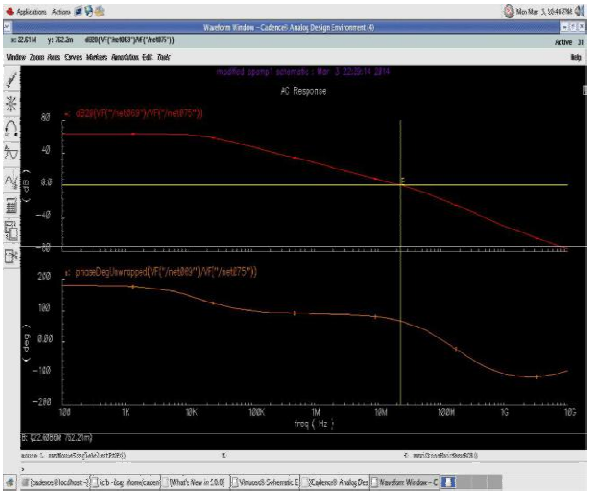

Fig. 9: Represents gain and frequency which give the gain bandwidth product

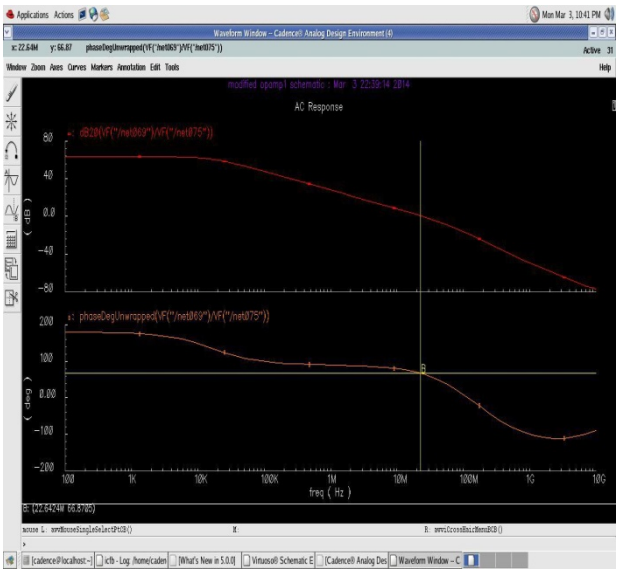

Fig. 10: Represents phase and frequency which will give phase margin.

4. CONCLUSION

A general approach for the design of two stage has been presented. The designed circuit allows calculated performance to be closely in agreement with the simulated one. To increase the gain and gain bandwidth product, a new circuit has been proposed. Calculation of profile parameters like Gain bandwidth product, Phase Margin, Gain, power dissipation is done by taking different values of coupling capacitor (C_C) and different ranges of ICMR. To improve Gain for the maximum value of ICMR i.e. at 1.6V, the value of Cc has decreased from 800fF to 500fF. So that the desired gain of 60dB is achieved using 500 fF coupling capacitor. Improvement in Phase Margin and GBW is done by recalculating values of W/L of transistors 1 and 2.

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